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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,242	10/16/2001	Karthisha S. Canagasaby	042390.P11916X	8029

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EXAMINER	
LUU, CUONG V	
ART UNIT	**PAPER NUMBER**
2128	

MAIL DATE	DELIVERY MODE
10/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/982,242	CANAGASABY ET AL.	
	Examiner	Art Unit	
	Cuong V. Luu	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 5-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2 and 5-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/26/2007 has been entered.

Claims 1-2 and 5-30 are pending. Claims 1-2 and 5-30 have been examined. Claims 1-2 and 5-30 have been rejected.

Response to Arguments

1. Applicant's arguments with respect to claims 1-2 and 5-30 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

2. Claim 10 is objected to for being identical to claim 9.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-2, 5-11, 15-18, and 22-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morrison et al (U.S. Patent 6,054,863).

3. As per claim 1, Morrison teaches a method comprising:

measuring first electrical characteristics of an interconnection, including generating a first graphical representation of an output of interconnection that is based, at least in part, on the first electrical characteristics (col. 2 lines 35-39 and lines 55-61); and

determining a test network having second electrical characteristics that include resistive and capacitive values such that the first electrical characteristics of the interconnection are approximated by the resistive and capacitive values of the test network, wherein determining the test network includes adjusting the resistive and capacitive values based on the first graphical representation wherein the determining includes creating a second graphical representation of an output of the test network based on the resistive and capacitive values that approximates the first graphical representation of the output of the interconnection (col. 5 lines 30-43, col. 7 lines 59-64.) within a specified tolerance (tolerance – design choice: making adjustable, See In re Stevens, 212 F.2d 197, 101 USPQ 284 (CCPA 1954)).

4. As per claim 2, Morrison teaches the test network is a resistive/capacitive network (col. 7 lines 59-64.)

5. As per claim 5, Morrison does not teach the tolerance of 10%. This number of 10% is a design choice. It would have been obvious to one of ordinary skill in the art to select a specified tolerance of any number including 10%.

6. As per claim 6, Morrison teaches the test network is a resistive network (col. 7 lines 59-64.)

7. As per claim 7, Morrison teaches the test network is a capacitive network (col. 7 lines 59-64.)

8. As per claim 8, Morrison teaches the test network is comprised of a plurality of resistive/capacitive networks (col. 5 lines 32-46).

9. As per claim 9, Morrison teaches connecting the resistive/capacitive network between a driver of a first input/output circuit and a receiver of a second input/output circuit (Fig. 2 and col. 4 lines 32-38).

10. As per claim 10, these limitations have already been discussed in claim 9. They are, therefore, rejected for the same reasons.

11. As per claim 11, variable resistors and capacitors have existed for decades. It would have been obvious to one of ordinary skill in the art to use them to implement a resistive/capacitive network in order to vary their values to approximate the interconnect.

12. As per claim 15, Morrison teaches an apparatus comprising:

an integrated circuit having at least one input/output ports, the at least one input/output ports having a driver and a receiver (fig. 3 and col. 5, lines 30-33. An integrated circuit, timers 24, inherently have at least one input/output ports having a driver and a receiver); and

a test network having second electrical characteristics that include resistive and capacitive values, the test network electrically coupling the driver and the receiver such that an input/output interface interconnection having first electrical characteristics may be emulated therewith, wherein the resistive and capacitive values are adjusted based on a first graphical representation of an output of the input/output interface interconnection that is generated based, at least in part, on the first electrical characteristics, wherein an output of the test network generates a second graphical representation based on the resistive and capacitive values that approximates the first graphical representation of the output of the input/output interface interconnection (these limitations have already been discussed in claim 1).

13. As per claim 16, these limitations have already been discussed in claim 2. They are, therefore, rejected for the same reasons.

14. As per claim 17, these limitations have already been discussed in claim 6. They are, therefore, rejected for the same reasons.

15. As per claim 18, these limitations have already been discussed in claim 7. They are, therefore, rejected for the same reasons.

16. As per claim 22, it is well known that a microprocessor has a timer. Therefore, it would have been obvious to one of ordinary skill in the art to use a timer, which is a part of a microprocessor. This limitation is, therefore, rejected.

17. As per claim 23, these limitations have already been discussed in claim 15. They are, therefore, rejected for the same reasons.

18. As per claim 24, these limitations have already been discussed in claim 2. They are, therefore, rejected for the same reasons.

19. As per claim 25, these limitations have already been discussed in claim 1. They are, therefore, rejected for the same reasons11.

20. As per claim 26, these limitations have already been discussed in claim 8. They are, therefore, rejected for the same reasons.

21. As per claim 27, these limitations have already been discussed in claim 8. They are, therefore, rejected for the same reasons.

22. As per claim 28, these limitations have already been discussed in claim 20. They are, therefore, rejected for the same reasons.

23. As per claim 29, these limitations have already been discussed in claim 14. They are, therefore, rejected for the same reasons.

24. As per claim 30, these limitations have already been discussed in claim 1. They are, therefore, rejected for the same reasons.

Claims 12-14 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morrison as applied to claims 11 and 16 above, and further in view of Neil et al (Principles of CMOS VLSI DESIGN A System Perspective, 2nd Edition, Addison-Wesley Publishing Company, 1993).

25. As per claim 12, Morrison does not teach the resistive/capacitive network is implemented on an integrated circuit chip.

However, Neil teaches implementing resistors and capacitors on an integrated circuit (pp. 134-135, section 3.3.2).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Morrison and Neil. Neil's teachings would have provided high-quality capacitor and resistors of variable characteristics (p. 130 section 3.3 1st paragraph of this section).

26. As per claim 13, it is well known to one of ordinary skill in the art a capacitor is can be implemented with gate capacitance. Therefore, it would have been obvious to one of ordinary skill in the art to use distributed gate capacitance to implement the capacitance.

27. As per claim 14, Morrison teaches implementing the resistive/capacitive network on a printed circuit board (col. 5lines 30-46).

28. As per claim 19, these limitations have already been discussed in claim 11. They are, therefore, rejected for the same reasons.

29. As per claim 20, these limitations have already been discussed in claim 12. They are, therefore, rejected for the same reasons.

30. As per claim 21, these limitations have already been discussed in claim 14. They are, therefore, rejected for the same reasons.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong V. Luu whose telephone number is 571-272-8572. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah, can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. An inquiry of a

general nature or relating to the status of this application should be directed to the TC2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CVL

FRED FERRIS
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100